

In the Claims:

Please amend claims 16 and 22 as follows:

1. (Original) A method for producing an adaptive bias current responsive to the input power of an RF amplifier, the method comprising steps of:  
accepting negative and positive input voltages of the RF amplifier;  
producing a differential current responsive to the negative and positive input voltages of the RF amplifier, wherein the differential current clips within the normal operational range of the RF amplifier; and  
filtering at least one harmonic from the differential current.
2. (Original) The method of claim 1, further comprising a step of subtracting quiescent bias current used to drive a circuit that conducts said step of producing from the differential current to produce the adaptive bias current that is responsive to the input power .
3. (Original) The method of claim 1, further comprising a step of multiplying the adaptive bias current.
4. (Original) The method of claim 3, wherein said step of multiplying comprises multiplying the adaptive bias current by a constant ratio.
5. (Original) The method of claim 4, wherein said step of multiplying further comprising a second stage multiplication that multiplies the adaptive bias current by a programmable ratio.
6. (Original) The method of claim 1, wherein said step of producing comprises:

generating a first current responsive to a negative voltage of the input power;  
generating a second current responsive to a positive voltage of the input power;  
and  
summing the first current and the second current to produce differential current.

7. (Original) The method of claim 1, wherein said step of filtering harmonics comprises low pass filtering the differential current responsive to the negative and positive input voltages of the RF amplifier.

8. (Original) The method of claim 7, wherein said step of low pass filtering is conducted with a pole frequency low enough to provide sufficient rejection of distortion components and high to respond to a signal envelope of the RF amplifier.

9. (Original) An adaptive bias current circuit for producing a bias current responsive to the input power of an RF amplifier, the bias current circuit comprising:  
current supply means for supplying a quiescent current; and  
differential power sensor means, biased by the quiescent current, for sensing the input power of the RF amplifier and for producing a bias current higher than the quiescent current when the input power reaches a high level, the bias current being responsive to the input power.

10. (Original) The circuit of claim 9, further comprising low pass filter means for filtering harmonics from the bias current.

11. (Original) The circuit of claim 10, further comprising first current multiplication means for multiplying the bias current.

12. (Original) The circuit of claim 11, further comprising second current multiplication means for multiplying the bias current by a programmable multiplication factor.

13. (Original) The circuit of claim 9, wherein said differential power means comprise:

means for producing a first current responsive to a positive voltage phase of the input power of the RF amplifier;

means for producing a second current responsive to a negative voltage phase of the input power of the RF amplifier; and

means for summing the first current and the second current to produce the bias current.

14. (Original) The circuit of claim 13, further comprising low pass filter means for filtering harmonics from the bias current.

15. (Original) The circuit of claim 14, further comprising current multiplication means for multiplying the bias current.

16. (Currently amended) An adaptive bias current circuit for producing a bias current responsive to the input power of an RF amplifier, the bias current circuit comprising:

a quiescent current bias supply circuit ~~(26)~~ generating a quiescent current;

a differential transistor pair ~~(28)~~ biased by the quiescent current, the differential transistor pair including a first transistor generating a first collector current responsive to a positive voltage phase of the input power of the RF amplifier and a second transistor generating a second collector current responsive to a positive voltage phase of the input

power of the RF amplifier, the quiescent current set to permit the first and second collector currents to clip when the input power of the RF amplifier reaches a predetermined level; and  
a current summer for summing the first and second collector currents to produce the bias current.

17. (Original) The circuit of claim 16, further comprising a low pass filter that receives and filters the bias current.

18. (Original) The circuit of claim 17, further comprising:  
a first current mirror to mirror the bias current;  
a subtractor to remove an amount of current corresponding to the quiescent current from the bias current; and  
a second current mirror to mirror and multiply the bias current.

19. (Original) The circuit of claim 18, further comprising a third current mirror that is programmable for multiplying the bias current.

20. (Original) An RF amplifier, the amplifier comprising:  
a current bias circuit in accordance with claim 16; and  
an amplifier circuit receiving the bias current from the current bias circuit.

21. (Original) The RF amplifier of claim 20, further comprising an output transistor amplifier in said amplifier circuit, said output transistor amplifier including a degeneration resistor.

22. (Currently amended) An adaptive bias current circuit comprising:  
a current supply ~~(26)~~ configured to supply a quiescent current; and

a differential power sensor configured to be biased by at least the quiescent current and to determine an input power of the RF amplifier and to generate a bias current larger than the quiescent current when the input power reaches a predetermined high level, the bias current being roughly proportional to the input power.